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**EDA CONSORTIUM PANEL: “WHAT CUSTOMERS WANT FOR
HARDWARE-SOFTWARE CO-DESIGN TOOLS”**

SAN JOSE, California, May 7, 2007 – The Electronic Design Automation (EDA) Consortium Emerging Companies Committee is hosting a panel at Cadence Design Systems in Chelmsford, MA entitled: “What Customers Want for Hardware-Software Co-Design Tools”. Panelists will present their current methodologies and suggest ideas for improving hardware-software co-design tools to help address upcoming challenges. The panel is moderated by Rich McAndrew, President of Siliance, Inc.

Panelists include:

- Bob Supnik, VP of Engineering, SiCortex: Developing high performance/low power multiprocessor chip set
- Vlad Kheyfets, Principal Engineer, Teradyne: SystemC modeling architect
- Sreeni Rao, Senior Manager, Analog Devices: Specializes in chip level and software integration for complex chips for hand-held devices and cell phones
- Ian Kersley, President of IPK Consulting: SystemC Expert

The event details are as follows:

When: May 10, 2007

Where: Cadence Design Systems
270 Billerica Road
Chelmsford, MA

Agenda: Reception 6 PM
Panel 7 PM
Q&A (30 Min.) 8 PM

Cost: No charge

Sponsors: EDA Consortium and Cadence Design Systems

Please reserve your seat by registering online at:

http://www.edac.org/invites/east_coast_meeting_07.htm.

About the EDA Consortium

The EDA Consortium is the international association of companies that provide tools and services that enable engineers to create the world's electronic products. EDA is the critical technology used to design electronics for the communications, computer, space technology, medical and industrial equipment and consumer electronics markets among others.

For more information about the EDA Consortium contact EDA Consortium, 111 West Saint John Street, Suite 220, San Jose, Calif. 95113, USA, office 408-287-3322, fax 408-283-5283 or visit www.edac.org.

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