NEWS RELEASE

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Analog/RF Chip Design Expert Helic Joins ESD Alliance
Notes Value in Being Part of Organization that Promotes System Design Ecosystem,
Fosters Networking

REDWOOD CITY, CALIF. — February 23, 2017 — Helic, a leading supplier of

Electronic Design Automation (EDA) software for crosstalk analysis and signoff of high-

frequency analog/RF and high-speed system-on-chip (SoC) design, today became a member of

the Electronic System Design Alliance (ESD Alliance) after its 10-member board approved

Helic's membership application.

"The ESD Alliance plays an important role in fostering the semiconductor design

ecosystem," notes Yorgos Koutsoyannopoulos, Helic's president and chief executive officer

(CEO). "Helic tools always have been interoperable with all key EDA tools/flows. The Helic

management sees great value in being part of an organization that brings the industry together to

collaborate on providing solutions to complex challenges such as crosstalk analysis and signoff

in high speed SoCs."

Helic noted the Alliance's networking activities such as the annual Phil Kaufman Award

dinner and ceremony, and emphasized the industry initiatives the EDA alliance sponsors, such as

Export, License Management and Interoperability, as important initiatives. It intends to be an active participant in all. According to Helic's Koutsoyannopoulos, also noteworthy is the Market Statistics Service (MSS), a tool that will support Helic's forecasting efforts.

"A hearty welcome to Helic," says Bob Smith, the ESD Alliance's executive director. "Crosstalk signoff is an area of great significance as demands for higher levels of integration of Analog/RF/Digital combined with higher speed/bandwidth as the industry moves into the era of the Internet of Things and high-speed networking. The Alliance will look toward Helic for insight into this emerging market."

About Helic

Helic of Santa Clara, Calif., develops and markets Electronic Design Automation (EDA) software that mitigates the risk of crosstalk in high-speed System on Chip (SoC) Designs and Analog/RF designs. Since 2000, its cutting-edge technology enables analog/RF and high-frequency IC design engineers to synthesize inductive devices and model electromagnetic and parasitic phenomena with accuracy, speed and seamless design flow interoperability. In the last few years, as frequency and bandwidth rise, Helic tools are used by SoC design teams from many of the top-10 semiconductor companies to analyze crosstalk in applications such as wireless communications, Internet of Things (IoT), computing, automotive and high-speed networking.

About the Electronic System Design Alliance

The Electronic System Design (ESD) Alliance, an international association of companies providing goods and services throughout the semiconductor design ecosystem, is a forum to address technical, marketing, economic and legislative issues affecting the entire industry. It acts as the central voice to communicate and promote the value of the semiconductor design industry

as a vital component of the global electronics industry. For more information about the ESD

Alliance, visit http://www.esd-alliance.org

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