CEO Perspective – ESD Alliance Committees: Worth the Cost of Membership
Dean Drako, President and CEO, IC Manage, Inc.

“That alone is worth the cost of membership.” This is a phrase I’ve heard many times in ESD Alliance Board of Directors meetings in response to the regular updates presented by many of the committee chairs.

While less visible than some of the high-profile events such as the Phil Kaufman Award Presentation and Dinner, the behind-the-scenes efforts of the technical committees are one of the key benefits of membership in the ESD Alliance.

The US Government is constantly introducing new regulations and updating existing ones. The fact that many of these updates do not disrupt the industry is a tribute to the efforts of the Export Committee, chaired by Larry Disenhof of Cadence Design Systems. Regularly, these new and updated regulations, while well meaning, contain wording that could have a significant negative impact on our industry. The ESD Alliance continuously monitors the regulatory agencies and has been effective in securing updates to the regulations, allowing the EDA and Semiconductor IP industries to continue to operate. Our industry alliance representatives can get results where individual companies do not have the same level of influence.

In addition to the industry-wide regulatory benefits, the committee has also provided valuable advice to smaller companies looking to avoid export related issues. A previous newsletter supplement highlighted two case stories where the committee was able to help companies navigate the complex set of government regulations. You can read the supplement at https://goo.gl/6xQkDx.

The License Management and Anti-Piracy Committee (LMA), chaired by Sashi Subramanian of Cadence Design Systems, continues to work diligently towards preventing the unauthorized — and unpaid — use of EDA tools, allowing members to recoup their significant development investment while protecting honest customers from competitors who did not pay for the tools needed to develop their products. Many EDA companies use Flexera for licensing. Presenting a unified voice regarding the inevitable bugs and other issues has been very valuable, especially allowing smaller Alliance members to benefit from the leverage of the larger members.

Moving forward, as the LMA Committee addresses issues of virtualization and the cloud, the committee provides the forum to discuss key issues with major customers, assuring the solutions we are currently investigating address their concerns, thus minimizing the issues associated with future licensing updates while continuing to protect each member’s intellectual property.

Lastly, the Interoperability Committee (better known as the OS Roadmap) chaired by Stephanie Chou of Keysight Technologies, continues to monitor the operating system landscape for the benefit of EDA vendors and users. The long, complex development cycles for EDA tools and chips presents unique challenges for operating system support and longevity. Given the costs for developing and supporting tools on each operating system, keeping the number of supported OSs to a reasonable number is important; determining which ones, however, is also complex. Committee members meet regularly amongst the members as well as OS vendors and publishes the resulting OS Roadmap to guide developers and customers. This can avoid costly issues associated with developing tools or chips on an operating system that reaches end-of-life before the development has been completed or installing an OS before the tools have been verified for that environment.

Each of these alone is “worth the cost of membership.” Members get all these benefits, and more.

For more information about the ESD Alliance and the benefits of its many initiatives, visit esd-alliance.org.
AMIQ EDA (Bucharest, Romania) provides productivity software tools that enable design and verification engineers to increase the speed and quality of new code development, simplify legacy code maintenance, accelerate language and methodology learning curves, and improve source code reliability.

Breker Verification Systems (San Jose, California) is the Portable Stimulus leader, adding GPS to your verification. Compliant with the upcoming Accellera Portable Stimulus standard, Breker automates the generation of target-specific, multi-threaded tests cases, by taking as inputs a single, executable Graph-based, Portable stimulus or spec of your verification intent, Shareable across platforms and projects.

Minima Processor Oy (Oulu, Finland) was founded in April 2016 to develop sub-threshold voltage processors based on technology developed by VTT Technical Research Centre of Finland Ltd. and the universities of Aalto and Turku. Minima was a founding partner in the RISC-V open hardware foundation.

Phil Kaufman Award Dinner, New ESD Alliance Members, DAC Design Infrastructure Alley
Bob Smith, Executive Director, ESD Alliance

It’s only February and the ESD Alliance already has plenty to be excited about.

Earlier this month, we co-hosted with IEEE Council on EDA (CEDA) the Phil Kaufman Award Ceremony and Dinner to honor Dr. Rob A. Rutenbar, senior vice chancellor for Research at the University of Pittsburgh (see supplement for photos). It was a great evening celebrating the recipient of the 2017 Phil Kaufman Award for Distinguished Contributions to Electronic System Design.

We added three new members in early 2018. First up was Minima Processor of Oulu, Finland. Next came AMIQ EDA of Bucharest, Romania. Lastly, we welcomed Breker Verification Systems, of San Jose, California. The products of each of these companies are noted above.

And, then there’s a trend we’re about to learn much more about. While the electronic system design ecosystem focused on SoCs and other complexity, an intriguing career evolution was going on quietly behind the scenes.

Anyone who worked in EDA in the past will remember the role of internal CAD manager whose massive — and likely stressful — responsibility was to maintain EDA tools inside on the IT network. Recently, they kept a low profile, though that’s all about to change as the renamed IT and design specialists step out from behind their sophisticated hardware and software that manage the design infrastructure and into the DAC spotlight.

DAC’s new Design Infrastructure Alley will be a tribute to these highly trained experts and their design technology infrastructures, a fundamental element for the creation and design of complex electronic systems and components. Their increased responsibilities range from keeping hardware and software for chip design working to managing computing bandwidth, availability, licensing, security and storage, and ensuring the design environment is optimized for fast turnaround and always-on availability. New innovation wouldn’t happen without them.

That’s why DAC fashioned the Design Infrastructure Alley, an opportunity for exhibitors and presenters to highlight a vital and expanding area of electronic product design. A dedicated Design-on-Cloud Pavilion theater will anchor the Design Infrastructure Alley and serve as a stage for presentations and panel discussions covering:

- License management
- Grid computing
- Storage management
- Data security
- Cloud computing

Credit for the Design Infrastructure Alley goes to Derek Magill, senior manager of IT at Qualcomm, and the ESD Alliance’s Paul Cohen and me who came up with the idea and worked with DAC to make it a reality. Derek also is chair of CELUG (Centralized Enterprise License User’s Group) that provides enterprise user input to the ESD Alliance’s license management committee.
DAC will be held June 24-28 at San Francisco’s Moscone West Center. DAC, the ESD Alliance and CELUG invite companies to exhibit in the Design Infrastructure Alley and promote this growing area of electronic product design. We also welcome professionals who manage the complex hardware/software infrastructure that keeps the electronic product design ecosystem running to participate.

For more information on DAC, its technical program and exhibits visit www.dac.com.

All told, now is a great time to be part of the ESD Alliance. If your company or you would like to join the ESD Alliance, please visit the ESD Alliance website to read about these active committees and our other ongoing initiatives. Or, contact me for more specifics on ROI or other justifications for joining. I can be reached at bob@esd-alliance.org

---

**Committee Updates**

**Export (Larry Disenhof, Cadence).** The Export Committee continues to monitor government activities and rulings that might have a significant impact on your business.

EDA technology, and the technology produced by most of our customers is considered “dual-use” and regulated by the Commerce Department, Bureau of Industry and Security (BIS). However the decision on control jurisdiction and what is restricted is made in coordination with representatives from three federal agencies: BIS, the State Department and DOD, along with input from industry. Each year, the agencies negotiate on increasing the export control thresholds to release older technologies from control. For example, without this annual review and release in the past decade, electronics below 28nm would be subject to ITAR (International Traffic in Arms Regulations) licensing due to the inherent “radiation hardened” nature of the devices that the shrinking geometry creates.

All three federal agencies have experienced a significant loss of personnel in the past year, and with that, an associated loss of institutional knowledge. There is concern that the personnel losses at these agencies will translate into lengthening times to process export licenses, and a slow-down in the annual review of technologies subject to restrictions. This year, we will join with other trade associations to monitor the situation and step in where needed to (hopefully) prevent unintended negative outcomes.

ESD Alliance member companies who need more information regarding these or other government issues potentially affecting your business should contact us.

**License Management & Anti-Piracy (LMA) (Sashi Subramanian, Cadence Design Systems).**

This quarter, the LMA committee continued to hold regular meetings to discuss matters of common interest. The LMA Committee had discussions around the Machine Certification development and the joint development agreement. Bob Smith discussed with the LMA Committee on how ESDA Member Companies can get the Machine Certification API/Library and Mark White (ESD Alliance Legal) reviewed the Machine Certification Program Framework and Joint Development agreement with the committee. The committee also discussed the need to have a Program Manager manage the logistics of the Machine Certification project.

Derek Magill, the chairperson of CELUG (Centralized Enterprise License Users Group), talked to us about the evolution of CELUG into a larger association that involves other aspects of Design IT — Grid Computing, Storage Management, Data Security, Cloud Computing — besides License Management. The latest news from DAC is there will be a new Design Infrastructure Alley, including exhibits and a new Design-on-Cloud Pavilion focused on all Design IT topics.

**Interoperability (Stephanie Chou, Keysight Technologies).** As the Electronic Systems Design market continues to evolve, the Interoperability Committee continues to explore additional factors that could impact the operation or the interoperability of tools or IP. Issues such as publishing OS version range and end-of-life guidelines, virtual machines, CPUs, forward/backward compatibility of OS versions, compilers, remote access tools, and container technology are among the most prominent candidates to consider.

We will once again be meeting with representatives of operating system vendors to discuss their development and support plans. This information will continue to be used to update and enhance the OS Roadmap.

As always, you can find the latest OS Roadmap on the ESD Alliance web site, esd-alliance.org.
Market Statistics Service (MSS): (Paul Cohen, ESD Alliance). The ESD Alliance’s MSS report captures EDA, semiconductor IP and services revenue data reported in complete confidence by companies providing these products and services and organizes it into a published report available to members. The most recent report, covering through Q3, 2017, shows quarterly industry revenue up 8% compared to Q3, 2016 on revenues of $2.3 billion. The report includes historical revenue data by quarter organized by detailed product categories and geographic regions. The report provides valuable data to help guide member companies’ business decisions. An overview is available in the MSS Newsletter, available at esd-alliance.org.

Emerging Companies (Steve Pollock, Sanida, Inc.). The Emerging Companies Committee continues to hold informative events on topics of interest to the electronic design ecosystem. We are busy planning several events for the spring, including a workshop on digital marketing for our member companies presented by Alliance member OneSpin, and the continuation of Jim Hogan’s series on the Cognitive Computing Era, in cooperation with San Jose State University. Check the Alliance web site, esd-alliance.org, for details! Recordings of past events are available in the ESD Alliance media library.

Tradeshow (Graham Bell, Uniquify). The committee represents the interests of ESD Alliance companies at the Design Automation Conference (DAC) and Design Automation and Test Europe (DATE).

The 55th DAC is coming back to San Francisco and will be a great showcase for ESD Alliance companies and their products, as well as an opportunity to hear a wide variety of technical papers. This year, it showcases exhibits and presentations centered on information technology (IT) infrastructure, a crucial element in the creation of electronic systems and components. A dedicated Design-on-Cloud Pavilion will be part of the new Design Infrastructure Alley that focuses on: License management, Grid computing, Storage management, Data security, and Cloud computing.

DAC invites all companies that are part of this vital and expanding area of the electronic product design industry to participate and exhibit in the Design Infrastructure Alley. DAC takes place in San Francisco, June 24 – 28, 2018.

DATE 2018 will be held March 19 through 23, 2018, at the International Congress Center, Dresden, Germany. The 21st DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. Two Special Days in the program will focus on areas bringing new challenges to the system design community: Future and Emerging Technologies and Designing Autonomous Systems, and each will have a full program of keynotes, panels, tutorials, and technical presentations. DATE includes more than 40 exhibitors and sponsors.

Follow us at:
Website: www.esd-alliance.org
ESD Alliance Bridging the Frontier blog: http://bit.ly/2oJUVzI
Twitter: @ESDAlliance
LinkedIn: https://www.linkedin.com/groups/8424092
Facebook: https://www.facebook.com/ESDAlliance
**Creative Collisions Describes This Year’s Phil Kaufman Award Ceremony and Dinner**
Bob Smith, Executive Director, ESD Alliance

The evening of February 8 was warm for early February in California’s Bay Area and warmth is the watchword for the Phil Kaufman Award Ceremony and Dinner. The electronic system design ecosystem turned out en masse to honor the popular entrepreneurial educator and good humored Dr. Rob A. Rutenbar, senior vice chancellor for Research at the University of Pittsburgh.

Dr. Rutenbar, or Rob as he’s known, might call the evening “Creative Collisions,” just as he titled his acceptance speech. The recipient of the 2017 Phil Kaufman Award for Distinguished Contributions to Electronic System Design was feted by family, friends and colleagues, and a host of former students in what was a great collision of creativity. Just consider the attendees who networked with each other — a collection of interesting and, in some cases, extraordinary people from business and academia. We even caught up with a former Phil Kaufman Award recipient or two.

As always, the evening was orchestrated by the ESD Alliance and the IEEE Council on EDA (CEDA). This year’s sponsors included Arm, Cadence, Mentor, a Siemens Business, PDF Solutions, Synopsys and ACM SigDA. It was held at The GlassHouse in downtown San Jose, a new venue for us, but a familiar landmark for San Jose Sharks fans because the SAP Center is close by.

Since it’s hard for me to describe in words how special the evening was, I turn over the rest of this page to photos ably taken by Paul Cohen, Ross Mehan and Julie Rogers. Even with their expert eyes, the photos might not fully capture the mood and conviviality or the warmth the industry has for Rob Rutenbar.
Dr. Martin Wong presented the tribute to Dr. Rutenbar.

Peter Rutenbar, Rob’s son, with Rob after the acceptance speech.

An audience of EDA industry people, including many of Rob’s former students, attended the award presentation and dinner.

1997 Phil Kaufman Award recipient Jim Solomon was among the previous honorees present to honor Rob. Steve Pollock and Ed Cheng are in the background.

IBM Fellow John Cohn, a former student, takes a selfie with Rob after presenting him with a medallion. Can you guess the significance?